REMARKS

Reconsideration and withdrawal of the outstanding rejections in consideration of this submission is respectfully requested.

At the outset, applicants note with appreciation the indication that the subject matter covered by dependent claims 4, 5, 7, 8, 10-12 and 14-16 are allowable and, moreover, that these claims would be formally allowed upon being re-presented in an appropriate self-contained format. It is submitted, however, in view of the re-presenting of original intervening claim 3 in an allowable independent claimed format, it is therefor not necessary to re-present the objected to claims which are dependent therefrom, i.e., claims 4, 5, 7, 8 and 10-12, in a separate self-contained format. Supportive discussion regarding this is further detailed hereinbelow. Also, as will be shown hereinbelow, applicants consider independent claim 13, in addition to all other currently pending claims, allowable over the art documents as cited in the outstanding rejections. Therefore, it is further unnecessary to re-present objected to claims 14-16, which depend therefrom, in a separate self-contained format.

There are now pending claims 2-20, of which claims 2-5 were amended. Claim 1 was canceled. Specifically, dependent claim was re-presented in an independent claim format, incorporating the subject matter of original base claim 1. Base intervening claim 3 was also re-presented as an independent claim, incorporating the subject matter of base claim 1. Additional revisions were implemented to claim 3 in consideration of removing an inadvertent earlier omission therefrom regarding the featured aspects directed to a "buffer amplifier" and, further, an additional "wherein" clause was added at the end of the claim for purposes of further clarifying the featured aspects therein. In this regard, part of the set forth

language in the last "wherein" clause of amended claim 3 is taken from the last "wherein" clause in claim 4 (see also claim 5). This of course relates to the controlled operation of the phase lock loop (PLL) of the FM transmitter. Incidentally, with regard to amended claim 3, minor editorial revisions were implemented therein. These revisions were generally limited to a rearranging of the subparagraphs, with regard to combining the subject matter of original claims 1 and 3, for purposes of improving the readability thereof. The adding of the expression regarding the "buffer amplifier" into claim 3 was effected strictly to remove an informality regarding the earlier inadvertent omission directed thereto. Examples of FM transmitters according to that covered by the present invention are given with regard to Figs. 1 and 2 of the drawings, although not limited thereto.

An FM transmitter according to the present invention is configured to control the start/idle of each of its component devices, including the buffer amplifier therein, thereby omitting the use of a sample-and-hold circuit for moving a PLL into open looped control. In this regard, the FM transmitter calls for a controller that controls the charging pump in the PLL to start/idle the FM modulation under the control of start/idle signals of both of the PLL and the buffer amplifier and outputs control signals for keeping the output of the charging pump in the high resistance state. (Page 3, line 22, to page 5, line 17, of the Specification.)

A featured aspect of the invention according to claim 2 concerns the outputting of a control signal by the controller (e.g., 13 in Fig. 1+ and 14 in Fig. 2+) in response to a start/idle signal of the PLL as well as a start/idle signal of the buffer amplifier (e.g., 9) in order to timely control the "charging pump" (e.g., 5) in consideration of controlling the switch status of the phase lock loop (PLL) between

open and closed. With regard to claim 3, further, the invention calls for the controller, in accordance with a signal regarding start and idle associated with the PLL as well as a start/idle signal of the buffer amplifier, to hold an output of the charging pump in a "high resistance state." The high resistance state can be seen with regard to Figs. 5/6 in which both the pull-up and pull-down portions of the CMOS arrangement remain in an off-state The invention according to claim 3 further calls for the PLL "to be held in a closed-loop control for a period from a start-up timing of the phase lock loop, and held in open loop control during other periods." This is further detailed with regard to claims 4 and 5. It is submitted, the invention according to claims 2 and 3+ could not have been rendered obvious in a manner as that alleged in the outstanding rejections. For the same and similar reasons, the invention according to claims 13+ and 17+ also could not have been rendered obvious as that alleged in the outstanding rejections directed thereto.

According to the outstanding Office Action, claims 1, 17 and 18 were rejected under 35 USC §103(a) over the admitted "prior art" in the background section of the Specification in view of Wentzler (USP 5, 151,665); and claims 2-3, 6, 9, 13, 19 and 20 were rejected under 35 USC §103(a) over the same combination of the admitted "prior art" in view of Wentzler, *supra*, and further in view of Juntunen et al (USP 6,163,711). As will be shown hereinbelow, the invention according to claims 2, 3+, 13+, and 17+ could not have been achievable in a manner as that argued in the outstanding rejections. Therefore, insofar as presently applicable, these rejections are traversed and reconsideration and withdrawal of the same is respectfully requested.

Wentzler disclosed a PLL with a charge pump having switchable resistances such as the first switchable resistance 13 and the second switchable resistance 14 shown in Fig. 2 thereof. According to the operation thereof, the first switchable resistance 13 switches from a resistance limited to resistor 11 to a different resistance effected by paralleling resistors 11 and 12 by the switching action of analog switch 15. Likewise, the second resistance 14 switches from that of resistor 21 to a resistance corresponding to the parallel resistance of resistors 21 and 22 as a result of the actuation of analog switch 25. (Fig. 2 and column 5, lines 32-52, in Wentzler.) However, Wentzler neither disclosed nor suggested a scheme by which the charge pump output 29 is controlled to switch the status of the phase lock loop between opened and closed, in contradistinction with that according to claims 2, 3+, 17+ and, also, according to claims 13+, although worded somewhat differently therefrom.

Wentzler, it is submitted, also neither disclosed nor suggested controlling a phase lock loop scheme so that it is held in closed loop control for a period from a start-up timing of the phase lock loop, e.g., through a timing delayed by a certain time from a start-up of the buffer amplifier, through a transmission timing of a preamble signal, and so on, and held in open loop control for other periods (e.g., see claims 3, 4, and 5).

With regard to Wentzler's PLL scheme, the first and second switched resistors 12 and 22 are connected to/disconnected from the charge pump 6a through the action of the first and second analog switches 15 and 25, respectively, in response to the charge pump control signal. Consistent with that stated above, this means that irrespective of whether the analog switches 15 and 25 remain on or off, the resistors

11 and 21 remain connected to the charging/discharging current action of the circuit. In other words, the first and second resistors 11 and 21 cannot be disconnected from the charge pump 6a noting that they remain connected to the charge pump 6a irrespective of whether the first and second switched resistors 12 and 22 are connected or disconnected to the pull-up and pull-down circuit portions, respectively. Accordingly, the emitter 10e of the source (pull-up) transistor 10 and the emitter 20e of the sink (pull-down) transistor 20 have a current driven therethrough, anytime. For this reason, it is submitted, Wentzler's charge pump cannot be held in an open loop control, any time.

As stated in the Office Action, the admitted prior art "does not disclose a charging pump in a phase lock loop and a controller to output a control signal to control an output of the charge pump." Even though Wentzler taught a phase lock loop scheme, Wentzler, however, failed to teach the combination of a phase lock loop, a controller and a buffer amplifier as that presently set forth in claims 2, 3+, 13+ and 17+. That is, as was shown hereinabove, contrary to that presently called for in claims 2, 3+, 13+ and 17+, Wentzler failed to teach the control of the switch status of the phase lock loop in the manner called for in claims 2, 3+, 13 and 17+. Juntunen et al was further cited for their teaching of a controller receiving a start/idle signal of the buffer amplifier. However, Juntunen, it submitted, does not overcome the other deficiencies in the admitted prior art as combined with Wentzler. Therefore, even if one of ordinary skill would have attempted to combine Juntunen et al's teachings with that of the admitted prior art as modified by Wentzler, the invention according to claims 2, 3+, 13+ and 17+ would still not have been realizable.

Therefore, in view of the amendments presented hereinabove together with these accompanying remarks, reconsideration and withdrawal of the outstanding rejections as well as favorable action on all of the presently pending claims and an early formal notification of allowability of the above-identified application is respectfully requested.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (Docket No. 501.41071X00), and please credit any excess fees to such deposit account.

Respectfully submitted,

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